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NS54335

6-V to 30-V Input, 3-A Output, Synchronous Step-Down DC-DC Converter

GENERAL DESCRIPTION

The NS54335 is synchronous converters with an input-voltage range of 6V to 30V. It has an integrated low-side switching FET that eliminates the need for an external diode which reduces component count. Efficiency is maximized through the integrated 90-mΩ and 65-mΩ MOSFETs, low I_Q and pulse skipping at light loads. Using the enable pin, the shutdown supply current is reduced to 2 µA. This step-down (buck) converter provides accurate regulation for a variety of loads with a well regulated voltage reference that is 1.5% over temperature.
Cycle-by-cycle current limiting on the high-side MOSFET protects the NS54335 in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. A low-side sinking current-limit turns off the low-side MOSFET to prevent excessive reverse current.
Hiccup protection is triggered if the overcurrent condition continues for longer than the preset time. Thermal shutdown disables the device when the die temperature exceeds the threshold and enables the device again after the built-in thermal hiccup time.

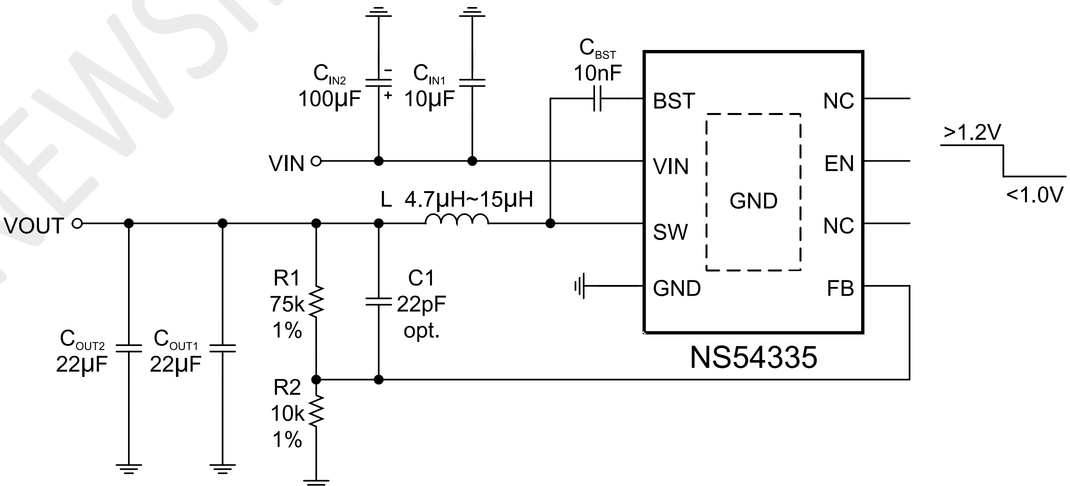
FEATURES

- Wide Input Voltage Range: 6V ~ 30V
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 90mΩ/65 mΩ
- 3A output current capability
- 500kHz Switching Frequency Minimize the External Components
- Internal 1.5-ms Soft-Start
- 0.6V/0.8V/0.925V Voltage Reference with ±0.8% Accuracy
- Current Mode Control
- Pulse Skipping for Light-Load Efficiency
- Hic-cup Mode Output Short Circuit Protection
- Compact Package: ESOP8
- Protection
  Under Voltage Protection (UVP)
  Over Voltage Protection (OVP)
  Over Current Protection (OCP)
  Short Circuit Protection (SCP)
  Over Thermal Protection (OTP)

APPLICATION

- Automotive Systems
- Network Terminal Equipment
- Security Monitoring Camera
- Printer Systems
- Industrial Power Systems
- Distributed Power Systems

TYPICAL APPLICATIONS



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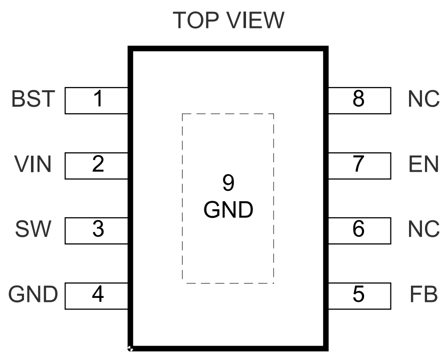
PIN CONFIGURATION



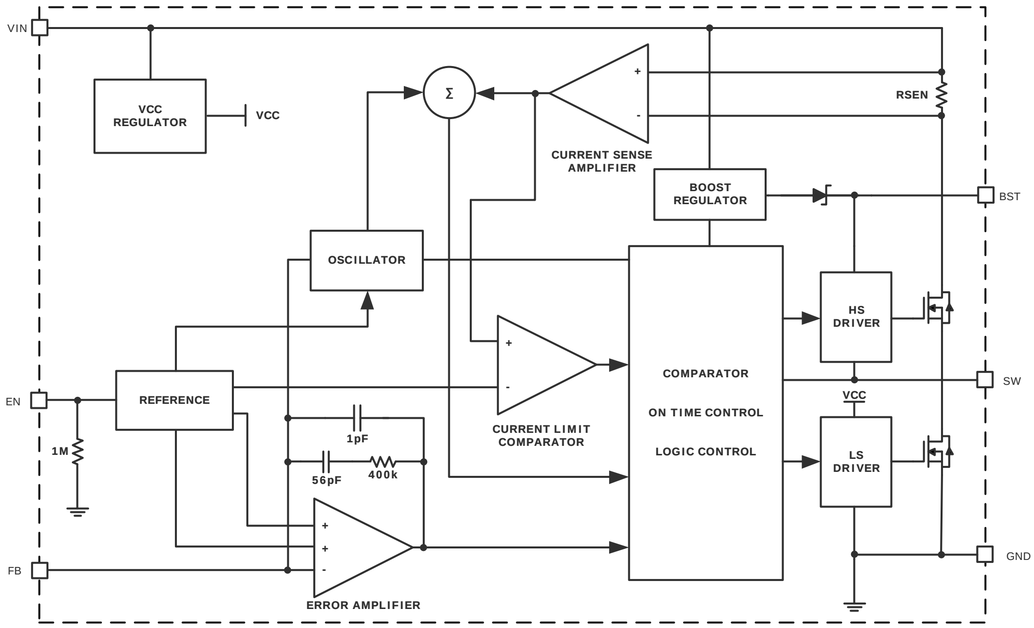
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	BST	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to SW pin with10nF ceramic cap.
2	VIN	Supply Voltage. The NS54335 operates from a 6V to 30V input rail. Requires C_{IN} to decouple the input rail. Connect using a wide PCB trace.
3	SW	Switch Output. Connect using a wide PCB trace.
4	GND	System Ground. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
5	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage
6	NC	NC
7	EN	Pull High to enable the NS54335. For automatic start-up, connect EN to IN using a resistor. Do not float.
8	NC	NC
9	GND	EPAD, connect to GND

ORDER INFORMATION

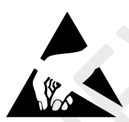
Model	Description	Package	Top Marking	Packaging	MPQ
NS54335A	PSM Buck, 6-30V, 3A, 500kHz, VFB 0.8V	ESOP8	54335A	Tape & Reel	3000
NS54335B	PSM Buck, 6-30V, 3A, 500kHz, VFB 0.925V	ESOP8	54335B	Tape & Reel	3000
NS54335C	PSM Buck, 6-30V, 3A, 500kHz, VFB 0.6V	ESOP8	54335C	Tape & Reel	3000

SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNIT
Supply Input Voltage	-0.3	38	V
SW,EN Voltage	-0.3	V_{IN} + 0.3	V
FB, BS-SW Voltage	-0.3	4	V
Junction Temperature Range	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Storage Temperature Range	-65	150	°C
Dynamic SW Voltage in 10ns Duration	GND-5V	V_{IN}+3V	V
Package Thermal Resistance θ_{JA}		42.1	°C/W
Package Thermal Resistance θ_{JC}		50.9	°C/W
HBM(Human Body Mode)		2	kV
MM(Machine Mode)		200	V



ESD(electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
Supply Input Voltage	6	30	V
Junction Temperature Range	-40	150	°C
Ambient Temperature Range	-40	85	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{OUT} = 5V, L = 10μH, C_{OUT} = 44μF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		6		30	V
Input OVP Threshold	V_{OVP}				38	V
Input OVP Hysteresis	V_{HYS}			4		V
Input UVP Threshold	V_{UVP}				5.3	V
Input UVP Hysteresis	V_{HYS}			0.6		V
Standby Supply Current	I_Q	I_{OUT}=0,V_{FB}=V_{REF}×105%		110		μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0		2		μA
EN Rising Threshold	V_{EN_R}			1.2		V
EN Falling Threshold	V_{EN_F}			1		V
Feedback Voltage	V_{REF}	NS54335A		0.8		V
		NS54335B		0.925		V
		NS54335C		0.6		V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	R_{DSON}			90		mΩ
Bottom FET RON	R_{DSON}			65		mΩ
Min ON Time	T_{ON_MIN}			50		ns
Min OFF Time	T_{OFF_MIN}			100		ns
Turn On Delay	T_{ON_DLY}	from EN high to SW start switching		180		μs
Soft-start Time	T_{SS}	V_{OUT} from 0 to 100%		1.5		ms
Switching Frequency	F_{SW}	V_{OUT}=3.3V, CCM		500		kHz
Top FET Current Limit	I_{LIM_TOP}			4.5		A
Bottom FET Current Limit	I_{LIM_BOT}			4.5		A
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}	Duty = 30%		15		℃

FUNCTIONAL DESCRIPTION

NS54335 is a high efficiency, 500kHz synchronous step-down DC/DC regulator, which is capable of delivering up to 3A load current. It can operate over a wide input voltage range from 6V to 30V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. NS54335 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection.

Soft Start

NS54335 has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps.
The typical soft-start time is 1.5ms.

OCP and SCP

If the high side power FET current gets higher than peak current limit threshold, the high side power FET will turn off and the low side power FET will turn on. If the low side FET current gets higher than valley current limit threshold, the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. So both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the regulation level, the output short is detected and the IC will operate in hic-cup mode. The hic-cup on time is 2.5ms and hic-cup off time is 9ms. If the hard short is removed, the IC will return to normal operation.

Enable and Adjusting UVLO

The EN pin has accurate rising and falling threshold, it provides programmable ON/OFF control by connecting an external resistor divider. Once the EN pin voltage exceeds the rising threshold, the device will start operation. If the EN pin voltage is pulled below the falling threshold, the regulator will stop switching and enter shutdown stat.

Detailed Design Procedure

Adjusting the Output Voltage

A resistor divider from the output node to the feedback pin sets the output voltage. Recommend using 1% tolerance or better divider resistors. Start with fixed value for the R1 resistor and use Equation to calculate R2.

To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the feedback input current are noticeable.

$$V_{OUT}=V_{FEEDBACK}\times\frac{R1+R2}{R2}$$

Select R1 value then

$$R2=R1\times\frac{V_{FEEDBACK}}{V_{OUT}-V_{FEEDBACK}}$$

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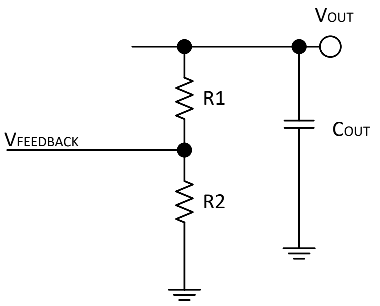


Inductor Selection

Use a inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation.

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times F_S}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)}=I_{LOAD}+\frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Input Capacitor Selection

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. For the best performance, use low ESR capacitors, such as ceramic capacitors with X5R or X7R dielectrics and small temperature coefficients. A 10µF capacitor is sufficient for most applications. The input capacitor requires an adequate ripple current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with:

$$I_{CIN}=I_{LOAD}\times\frac{\sqrt{V_{OUT}\times(V_{IN}-V_{OUT})}}{V_{IN}}$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, where:

$$I_{CIN}=\frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. Place a small, high-quality, ceramic capacitor (0.1µF) as close to the IC as possible when using electrolytic or tantalum capacitors. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with:

$$\Delta V_{IN}=\frac{I_{LOAD}}{F_S\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})$$

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_S\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times F_S\times C_{OUT}}\right)$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times F_S^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_S\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

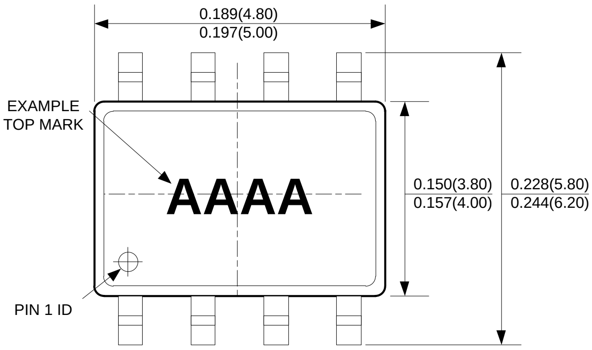
The characteristics of the output capacitor also affect the stability of the regulation system. The NS54335 can be optimized for a wide range of capacitance and ESR values.
For the best performance, it is recommended to use X5R or a better grade ceramic capacitor with 16V rating and more than 44μF capacitance.

Bootstrap Capacitor Selection
Connect a 100nF ceramic capacitor between the SW and BS pins for proper operation. Recommend using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 6.3V or higher voltage rating.

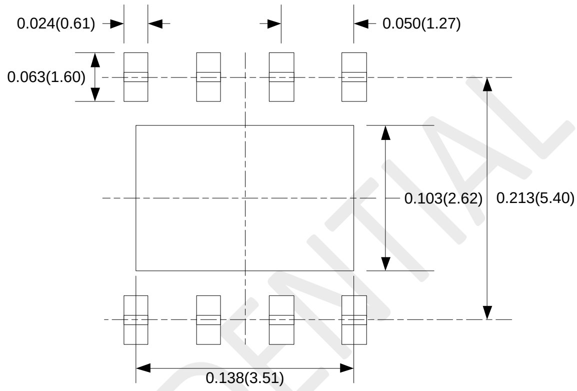
Layout Guidelines
PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.
1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator V_{IN} terminal, to the regulator SW terminal, to the inductor then out to the output capacitor C_{OUT} and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to C_{OUT} and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the V_{IN} terminal. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

PACKAGE

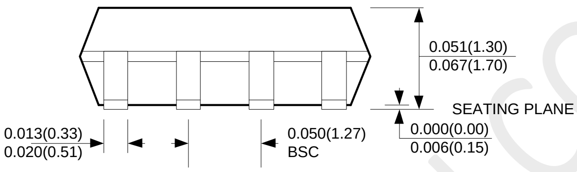
SOP8(EXPOSED PAD)



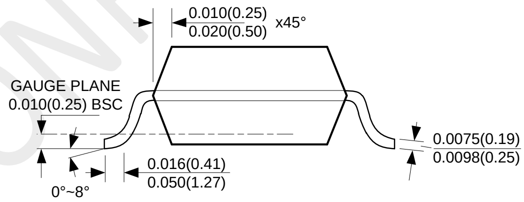
TOP VIEW



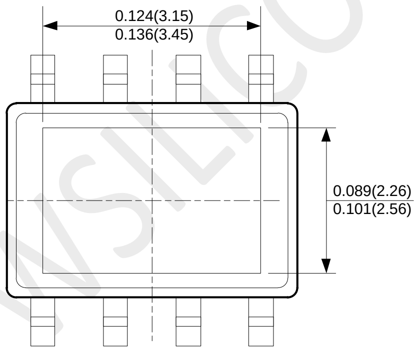
RECOMMENDED SOLDER PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.